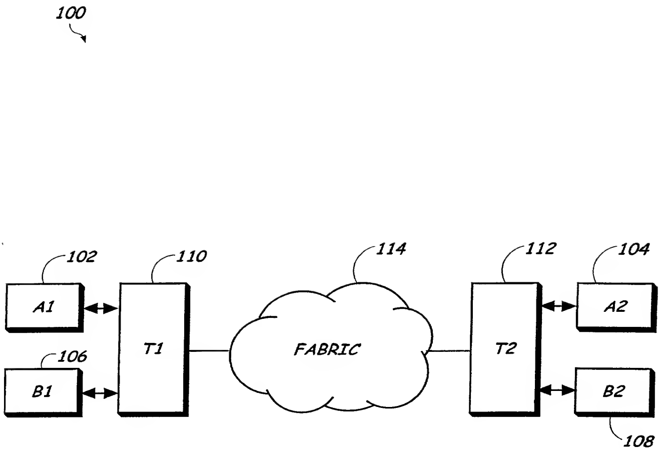

FIG. 1A

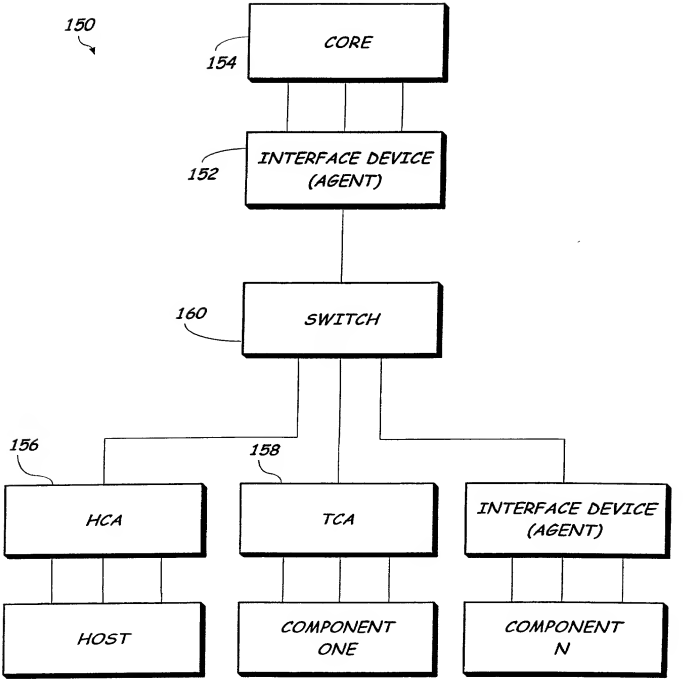
150
CORE
154
INTERFACE DEVICE
(AGENT)
152
SWITCH
160
156
158
HCA
TCA
INTERFACE DEVICE
(AGENT)
HOST
COMPONENT
ONE
COMPONENT
N

FIG. 1B

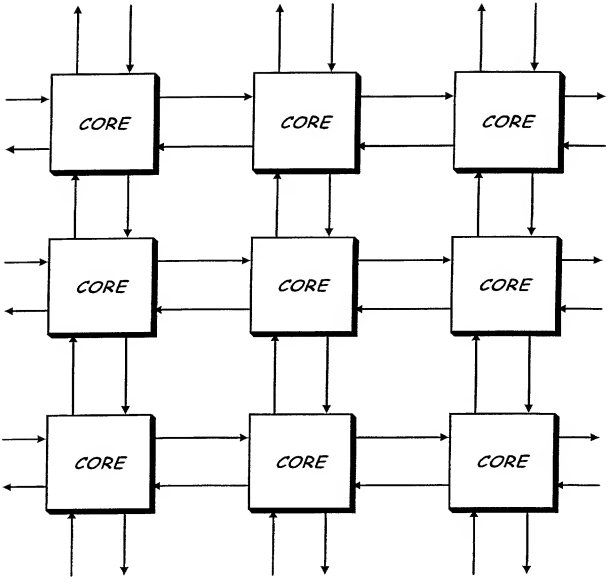

FIG. 1C

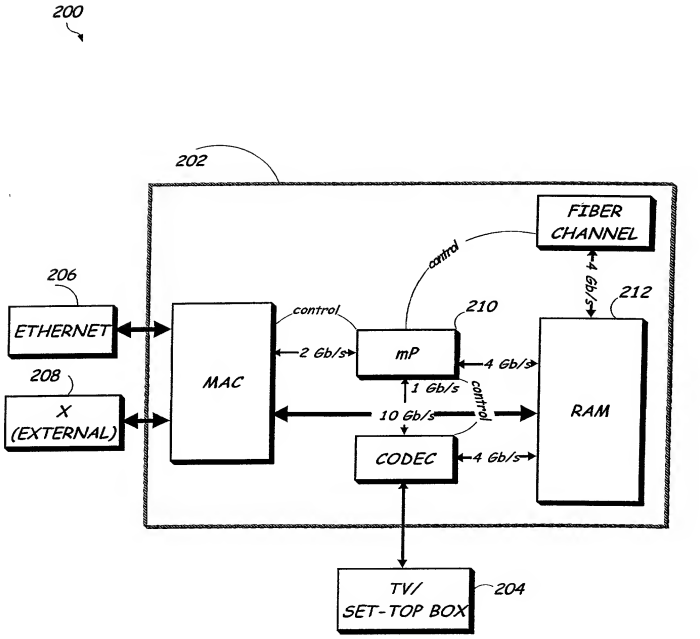
200
202
FIBER CHANNEL
control
4 Gb/s
212
206
ETHERNET
control
210
MAC
2 Gb/s
mP
4 Gb/s
208
X (EXTERNAL)
1 Gb/s
control
10 Gb/s
RAM
CODEC
4 Gb/s
TV/ SET-TOP BOX
204

FIG. 2

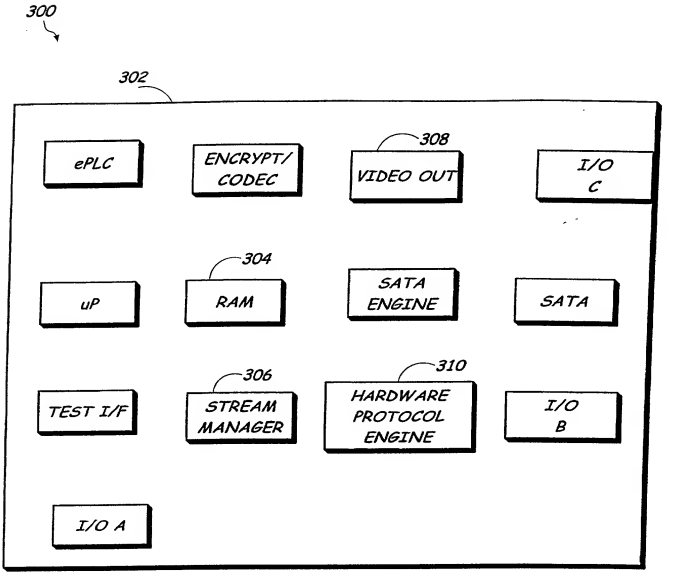
300
302
ePLC
ENCRYPT/
CODEC
308
VIDEO OUT
I/O
C
uP
304
RAM
SATA
ENGINE
SATA
TEST I/F
306
STREAM
MANAGER
310
HARDWARE
PROTOCOL
ENGINE
I/O
B
I/O A

FIG. 3

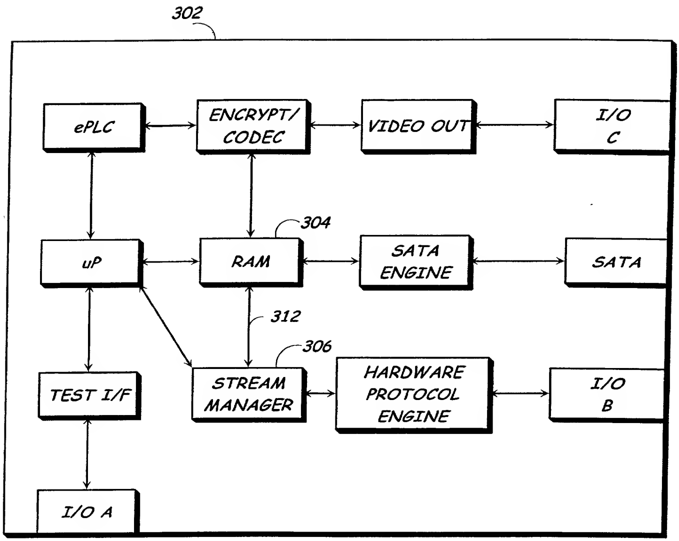
302
ePLC
ENCRYPT/ CODEC
VIDEO OUT
I/O C
304
uP
RAM
SATA ENGINE
SATA
312
306
TEST I/F
STREAM MANAGER
HARDWARE PROTOCOL ENGINE
I/O B
I/O A

FIG. 4

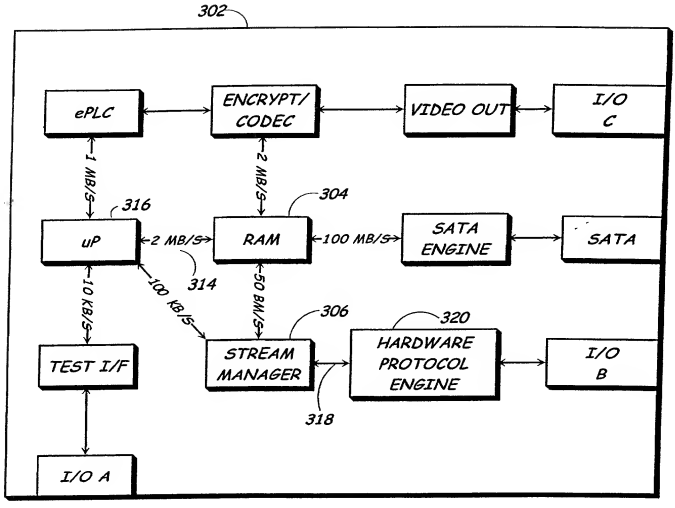
302
ePLC
ENCRYPT/
CODEC
VIDEO OUT
I/O
C
1 MB/S
2 MB/S
316
304
uP
2 MB/S
RAM
100 MB/S
SATA
ENGINE
SATA
314
10 KB/S
100 KB/S
50 BM/S
306
320
TEST I/F
STREAM
MANAGER
HARDWARE
PROTOCOL
ENGINE
I/O
B
318
I/O A

FIG. 5

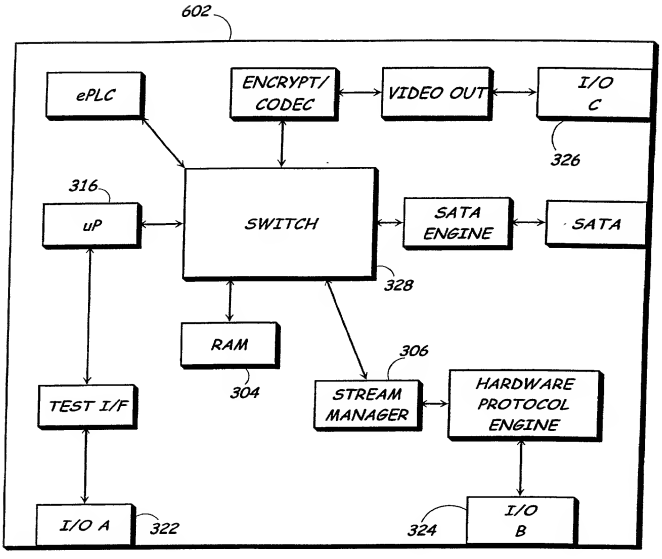
602
ePLC
ENCRYPT/
CODEC
VIDEO OUT
I/O
C
326
316
uP
SWITCH
SATA
ENGINE
SATA
328
RAM
304
306
TEST I/F
STREAM
MANAGER
HARDWARE
PROTOCOL
ENGINE
I/O A
322
324
I/O
B

FIG. 6

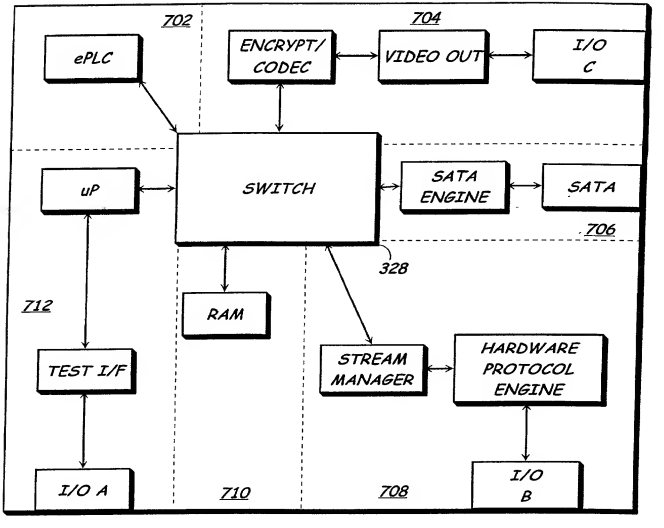
702
704
ePLC
ENCRYPT/
CODEC
VIDEO OUT
I/O
C
uP
SWITCH
SATA
ENGINE
SATA
706
328
712
RAM
TEST I/F
STREAM
MANAGER
HARDWARE
PROTOCOL
ENGINE
I/O A
710
708
I/O
B

FIG. 7

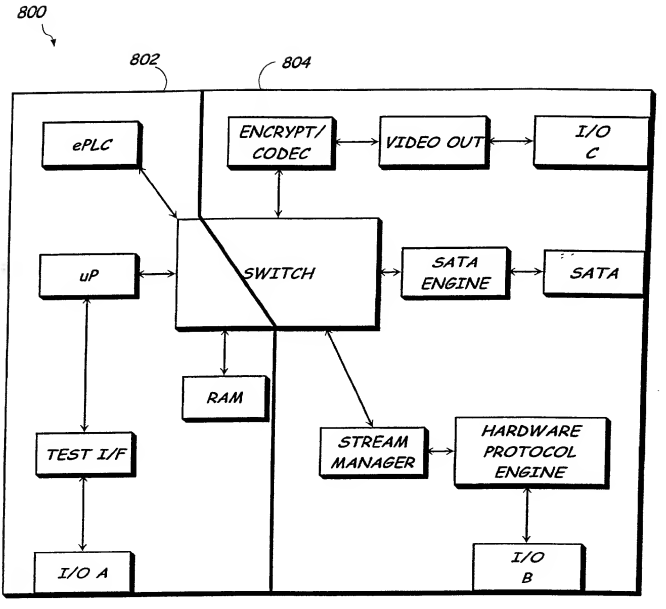
800
802
804
ePLC
ENCRYPT/
CODEC
VIDEO OUT
I/O
C
uP
SWITCH
SATA
ENGINE
SATA
RAM
TEST I/F
STREAM
MANAGER
HARDWARE
PROTOCOL
ENGINE
I/O A
I/O
B

FIG. 8

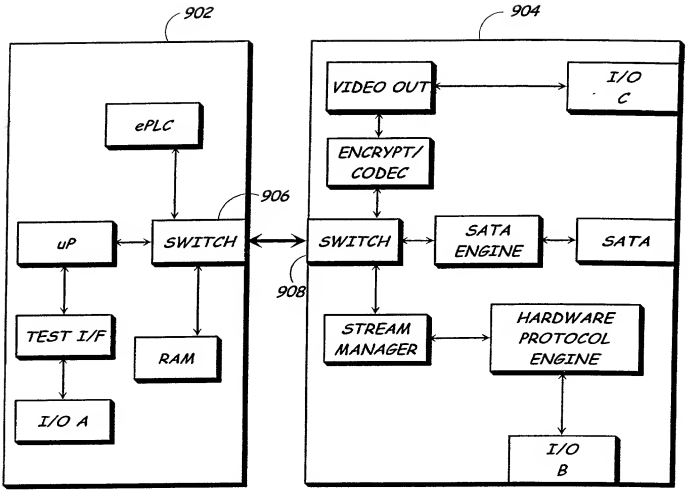
900
902
904
ePLC
VIDEO OUT
I/O C
ENCRYPT/ CODEC
906
uP
SWITCH
SWITCH
SATA ENGINE
SATA
908
TEST I/F
RAM
STREAM MANAGER
HARDWARE PROTOCOL ENGINE
I/O A
I/O B

FIG. 9

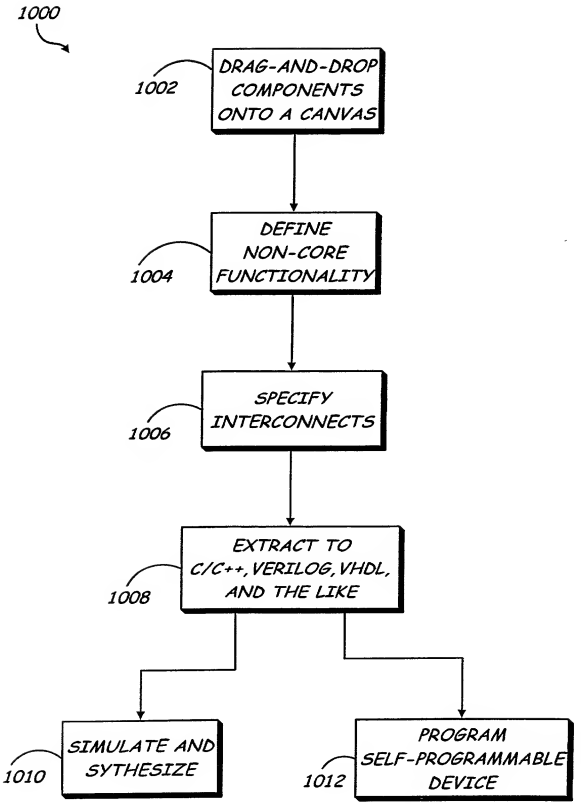
1000
1002
DRAG-AND-DROP COMPONENTS ONTO A CANVAS
1004
DEFINE NON-CORE FUNCTIONALITY
1006
SPECIFY INTERCONNECTS
1008
EXTRACT TO C/C++, VERILOG, VHDL, AND THE LIKE
1010
SIMULATE AND SYTHESIZE
1012
PROGRAM SELF-PROGRAMMABLE DEVICE

FIG. 10

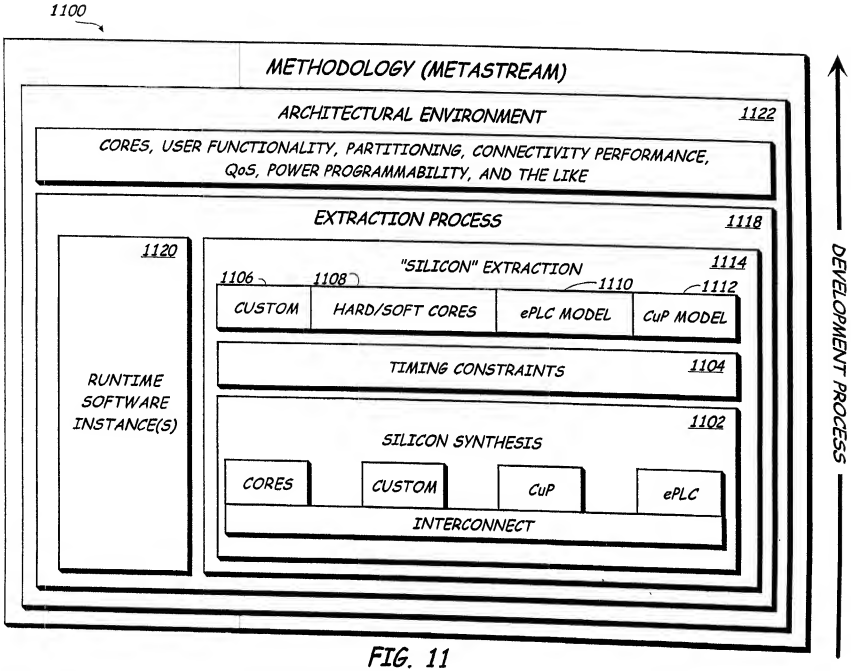
1100
METHODOLOGY (METASTREAM)
ARCHITECTURAL ENVIRONMENT
1122
CORES, USER FUNCTIONALITY, PARTITIONING, CONNECTIVITY PERFORMANCE, QoS, POWER PROGRAMMABILITY, AND THE LIKE
EXTRACTION PROCESS
1118
1120
RUNTIME SOFTWARE INSTANCE(S)
"SILICON" EXTRACTION
1114
1106
1108
1110
1112
CUSTOM
HARD/SOFT CORES
ePLC MODEL
CuP MODEL
TIMING CONSTRAINTS
1104
1102
SILICON SYNTHESIS
CORES
CUSTOM
CuP
ePLC
INTERCONNECT
DEVELOPMENT PROCESS

FIG. 11